**COURSE OUTLINE**

**Course Code: CSE205**

**Course Title: Digital Logic Design**

**Level/Term: 2/1 Section: A/B**

**Academic Session: January 2018**

**Course Teacher(s):**

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| **Name:** | **Office/Room:** | **E-mail and Telephone: (optional)** |
| Dr. Mahmuda Naznin  *Professor* | 318 | mahmudanaznin@cse.buet.ac.bd |
| Dr. Abdullah Adnan  *Assistant Professor* | 311 | adnan@cse.buet.ac.bd |

**Course Outline:**

Digital logic: Boolean algebra, De Morgan's Theorems, logic gates and their truth tables, canonical forms, combinational logic circuits, minimization techniques; Arithmetic and data handling logic circuits, decoders and encoders, multiplexers and de-multiplexers; Combinational circuit design; Flip-flops, race around problems; Counters: asynchronous counters, synchronous counters and their applications; PLA design; Synchronous and asynchronous logic design; State diagram, Mealy and Moore machines; State minimizations and assignments; Pulse mode logic; Fundamental mode design.

**Learning Outcomes/Objectives:**

After undergoing this course, students should be able to:

1. Understand number systems and binarylogic for representing information in digital systems.
2. Simplify circuits with different methods and reduce the overall cost of the design.
3. Define combinational circuits and design applications with them.
4. Understand sequential circuits and perform simple projects with them.
5. Derive the state-machine analysis or synthesis and perform simple projects with a few flip-flops.

**Assessment**

ClassTests/Assignments/ Projects: 20%

Attendance: 10 %

Term final: 70%

**Text and Reference books:**

a. Digital Design (5th edition), M. Morris Mano, Michael D. Ciletti

b. Digital Design: A Pragmatic Approach, Everett L. Johnson, Mohammad A. Karim

**Weekly schedule:**

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| **Week** | **Topics** | **Teacher’s Initial** |
| Week 1 | Introduction to Digital Logic Design  Digital Systems and Binary Numbers | MN |
| Week 2 | Digital Systems and Binary Numbers  Boolean Algebra and Logic Gates | MN |
| Week 3 | Boolean Algebra and Logic Gates | MN |
| Week 4 | Gate Level Minimization | MN |
| Week 5 | Gate Level Minimization Contd. | MN |
| Week 6 | Combinational Logic | MN |
| Week 7 | Combinational Logic Contd. | MN |
| Week 8 | Synchronous Sequential Logic | AA |
| Week 9 | Synchronous Sequential Logic | AA |
| Week 10 | Registers and Counters | AA |
| Week 11 | Registers and Counters | AA |
| Week 12 | Asynchronous Sequential Logic | AA |
| Week 13 | Asynchronous Sequential Logic | AA |
| Week 14 | PLA Design | AA |

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| Prepared by : |  |
| Name: Dr. Mahmuda Naznin  Signature:  Date: | Name: Dr. Md. Abdullah Adnan  Signature:  Date: |